

REMARKS

Applicant thanks the Examiner for indicating that claims 9-14 are allowable and for indicating that claims 6-8 (now canceled) contained allowable subject matter. Applicant also thanks the Examiner for considering the references cited in the IDSs submitted on December 31, 2001 and May 7, 2003. However, Applicants note that a fully initialed PTO 1449 form for the IDS submitted on December 31, 2001 which shows that the references have been considered has not been received by the Applicants. Accordingly, Applicants respectfully request the Examiner to take appropriate steps to ensure all of the considered references are cited on the issued patent, such as providing a fully initialed PTO 1449 form if appropriate.

I. Introduction

Claims 9-14 and 18-30 are pending in the above application.

Claims 9-14 stand allowed.

Claims 18-30 are newly added.

Claims 9, 11, 18 and 23 are the independent claims.

II. Amendments

Claims 1-8 and 15-17 have been canceled without prejudice or disclaimer. Accordingly, the rejections thereon are believed to be moot. Claims 18-30 are newly added.

No new matter has been added.

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III. New Claims

New claims 18-30 are believed to be patentable because they are believed to recite combinations of elements which are not disclosed or suggested by the prior art. For the Examiner's convenience, the Park (U.S. Pub. 2001/0043176A1) reference and Sasaki (U.S. Pat. 6,221,849) reference is discussed below.

Park (US 2001/0043176)

Park fails to disclose or suggest that each of the plurality of in-chip reference voltage wire units directly connects an input-side pad unit to an output-side pad unit on the corresponding driver circuit devices. Thus, Park does not disclose or suggest the features of the invention recited by the combination of elements in new claim 18 or 23.

Sasaki et al. (USP 6,211,849; "Sasaki")

Sasaki discloses a plurality of Driver ICs 1, and inter-module wirings 10 which is provided between the plurality of Drivers ICs 1 and connects an input pad portion 2 and an output pad portion 3 (see Fig. 3). Sasaki fails to disclose or suggest a plurality of in-chip reference voltage wire units directly connecting the input pad portion 2 and the output pad portion 3 on one of the plurality of Driver ICs 1. Fig. 4 of Sasaki shows that a latch circuit 5, 7 or a duty cycle regulator 6 is provided between the input pad portion 2 and the output pad portion 3. In addition, Fig. 12 shows that a voltage stabilizer 12 is provided between the power input pad portion 11 and the power output pad portion 13. When a reference voltage is applied to the aforesaid configuration, for example to an analog buffer, the reference voltage, which is obtained by connecting sequentially the plurality of Driver ICs 1, varies due to an offset voltage of the analog buffer, causing a visual problem such as mottling of the liquid crystal element.

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On the other hand, in the Applicant's configuration, since each of the plurality of in-chip reference voltage wire units directly connects the input-side pad unit and the output-side pad unit on the corresponding driver circuit devices. As a result, the reference voltage can be equally supplied between the plurality of driver circuit devices.

VI. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
MCDERMOTT, WILL & EMERY

Lawrence T. Cullen
Registration No. 44,489

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 LTC:MWE
Facsimile: (202) 756-8087
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